REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested.

In the present Office Action, Claim 15 stands rejected under 35 U.S.C. §112, second paragraph, as allegedly lacking antecedent basis for the phrase "said source/drain extension and halo implant regions".

In response, applicants have deleted Claim 15 and added Claim 21. Support for newly added Claim 21 is found at page 10, line 24 to page 11, line 4. Applicants submit that the above amendment overcome the §112, second paragraph rejection, therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 10 to 12 and 14 to 20 stand rejected under 35 U.S.C. §103(a), as allegedly obvious over U.S. Patent No. 6,010,921 to Soutome (hereinafter "Soutome") in view of Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Second Edition, Lattice Press, 2000, pages 202, 421-423 and 833-834 (hereinafter "Wolf"). Claim 13 stands rejected under 35 U.S.C. §103(a), as allegedly obvious over Soutome in view of Wolf, and further in view of U.S. Patent No. 5,685,951 to Torek et al. (hereinafter "Torek et al.").

More specifically, the Examiner asserts that Soutome discloses the semiconductor method substantially as claimed. Although Soutome fails to show the method comprising the step of forming sacrificial nitride spacers on portion of said gate dielectric, the Examiner avers that Wolf teaches the conventionally known properties of

silicon nitride material. Thus, the Examiner alleges that it would have been obvious to one skilled in the art to substitute, the method comprising the step of forming sacrificial nitride spacers on portion of said gate dielectric in the method of Soutome, according to the teaching of Wolf, with the motivation that the silicon nitride is conventionally used as sidewall spacers for MOSFET devices.

Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness as discussed below.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the cited reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the reference, not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Soutome and Wolf, solely or in combination, do not teach or remotely suggest the claimed method.

Soutome discloses a method of fabricating a recessed channel CMOS device comprising the steps of: providing a patterned oxide layer 5 over an SOI layer 3, said patterned oxide layer exposing a portion of said SOI layer; thinning the exposed portion of the SOI layer to form a recessed channel region; forming sacrificial spacers 8 on portion of said gate dielectric; forming a gate dielectric oxide film 9 on said recessed channel region; forming a gate electrode 10 on the other portions of the gate dielectric not

containing said sacrificial spacers; recessing the oxide layer exposing SOI layer abutting the recessed channel region; removing the sacrificial spacers 8; forming a source/drain diffusion regions 19 in said exposed SOI layer abutting the recessed channel region; and forming extension implant regions 18 in said SOI layer (column 7, line 1 to 67, and column 8, line 1 to 18). Notably, the sacrificial spacer 8 is formed prior to the formation of the gate dielectric oxide film 9 and is removed prior to the formation of the source/drain diffusion regions 19.

In contrast, the present invention teaches a method of fabricating a recessed CMOS device comprising the steps of: providing a patterned providing a patterned oxide layer over an SOI layer, said patterned oxide layer exposing a portion of said SOI layer; thinning the exposed portion of the SOI layer to form a recessed channel region; forming a gate dielectric on said recessed channel region; forming sacrificial nitride spacers on portions of said gate dielectric so as to protect exposed walls of said SOI layer and said oxide layer; forming a gate conductor on other portions of the gate dielectric not containing said sacrificial nitride spacers; recessing the oxide layer exposing SOI layer abutting the recessed channel region; forming source/drain diffusion regions in said exposed SOI layer abutting the recessed channel region; removing the sacrificial nitride spacers; and forming extension implant regions in said SOI layer such that said extension implant regions have an abrupt lateral profile and are located beneath the gate conductor. Notably, the sacrificial nitride spacers are formed **after** the formation of the gate dielectric oxide and are removed **after** the formation of the source/drain diffusion regions.

In view of the above, the sequences of performing the steps disclosed in Soutome and the inventive method are different. In particular, the sacrificial spacer in the present inventive method is present during the fabrication of the recessed channel and the source/drain regions, while the sacrificial spacer in Soutome method is removed prior to the formation of the source/drain regions. The present application further teaches that the objects and advantages of the present invention are achieved by utilizing a method wherein sacrificial spacers are present during the fabrication of the recessed channel and the source/drain regions, but are removed just prior to formation of the extension implant regions. This ensures that the extension implant regions as well as the halo implant regions have an abrupt lateral profile that extends beneath the edges of the gate region of the MOSFET device (page 3, line 15 to 21). Thus, applicants submit that the inventive method is different from and superior over the Soutome method.

Although Wolf teaches the conventionally known properties of silicon nitride material that Soutome fails to show, Wolf does not teach or remotely suggest the presence of sacrificial spacers during the fabrication of the recessed channel and the source/drain regions.

Therefore, Soutome and Wolf, solely or in combination, fail to teach or remotely suggest all the limitations of Claim 10 and dependant claims thereof.

Further, there is no motivation in Soutome and Wolf which suggests modifying the disclosed Soutome method in such a way to remove sacrificial spacers after formation of the source/drain regions and just prior to formation of the extension implant regions. Therefore, applicants respectfully submit that one skilled in the art, in view of the disclosed method in Soutome and the teaching of nitride properties in Wolf,

would not readily envision a method of fabricating a recessed CMOS device wherein sacrificial spacers are present during the fabrication of the recessed channel and the source/drain regions, but are removed just prior to formation of the extension implant region, as the present invention does.

Thus, applicants respectfully submit that Soutome and Wolf do not render Claim 10 and dependant claims thereof obvious.

Inasmuch as the principle references, i.e., Soutome and Wolf, spurring each of the obviousness rejections do not teach or suggest the claimed limitations of the present invention, the other applied reference, namely, Torek et al., is further removed from the claimed invention as is evident by including the reference in rejecting an aspect of applicants' dependent claim. Torek et al. do not teach or remotely suggest applicants' claimed method wherein sacrificial spacers are present during the fabrication of the recessed channel and the source/drain regions, but are removed just prior to formation of the extension implant regions. Applicants therefore respectfully submit that the §103 rejection over Soutome in view of Wolf, and further in view of Torek et al. also fails because the above references, whether used solely or in combination, do not teach or suggest the claimed method of the present invention.

The various §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed method to arrive at the present inventive method. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above.

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remark, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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